

1 ~~12. 22.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ~~7~~
 ~~27~~,
4 wherein said flash memory is an NOR type flash memory.

1 ~~13.~~
 ~~23.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ~~1~~
 ~~11~~,
4 wherein each of said at least one pair of laminating
5 structure bodies constitutes a memory cell of a flash
6 memory, and writing into said memory cell is carried out by
7 injecting a charge into said floating gate electrode.

1 ~~14.~~
 ~~24.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ~~13~~
 ~~23~~,
4 wherein said flash memory is an NOR type flash memory.

REMARKS

In response to the outstanding restriction
requirement, Applicants hereby elect the invention II
(Claims 11-21) for examination. Claims 22-24 newly
presented herein are directed to the elected invention and